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First Named Inventor	Pai-Hung Pan
Art Unit	2823
Examiner Name	G. Fourson III
Attorney Docket Number	2269-2919.4US (96-0499.01/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Reply Brief in response to Examiner's Answer dated January 18, 2007
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

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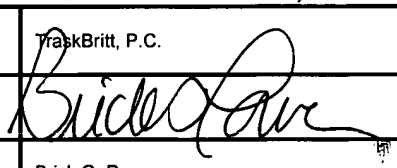
Signature			
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Date	March 19, 2007	Reg. No.	38,581

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Pai-Hung Pan

Serial No.: 09/072,959

Filed: May 5, 1998

For: TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

Confirmation No.: 7136

Examiner: G. Fourson III

Group Art Unit: 2823

Attorney Docket No.: 2269-2919.4US

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REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This Reply Brief is being filed in the format required by 37 C.F.R. § 41.41. As March 18, 2007, fell on a Sunday, this REPLY BRIEF, which is being submitted on Monday, March 19, 2007, should be deemed to have been filed within two months of the January 18, 2007, mailing date of Examiner's Answer in the above-referenced appeal. 37 C.F.R. § 1.7.

(VII) ARGUMENT

C. ANALYSIS

1. TSAI IN VIEW OF LANCASTER

It is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37.

First, it is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine teachings from Tsai and Lancaster in the manner that has been asserted.

Lancaster teaches a process for fabricating transistor gates within trenches. In that process, a silicon nitride layer 53, which acts as an etch stop (col. 3, line 19) and as part of a mask (col. 3, lines 39-40), remains in place as trenches 56 that have been formed through apertures of the mask 55 are lined with a sacrificial oxide 52a (col. 3, lines 41-45). The sacrificial oxide 52a is formed before removing the silicon nitride layer 53 because the etchants that are used to remove the silicon nitride layer 53 may also etch silicon surfaces that would otherwise be exposed within the trenches 56. Col. 3, lines 41-45. Once the silicon nitride layer 53 has been removed, the sacrificial oxide 52a is also removed (col. 3, lines 46-49), and transistor gate is fabricated.

In Tsai, which teaches processes for fabricating shallow trench isolation (STI) structures, edges of a silicon nitride layer 34a, which acts as a CMP stop (col. 3, lines 55-56), are etched back as silicon within a trench is exposed. FIG. 3E. Notably, Lancaster and Tsai teach that phosphoric acid may be used to remove silicon nitride. *See,* Lancaster, col. 3, lines 41-42; Tsai, col. 3, lines 21-23. Tsai teaches that any defects that occur as the edges of the silicon nitride

layer 34A are etched back may simply be relieved by lining the trenches 38A with side wall oxidation 39. Col. 3, lines 34-37.

According to the Examiner, it "would have been expected by one of ordinary skill in the art to protect the trenches during etching as disclosed by Lancaster and to prevent the defect formation disclosed by Tsai et al rendering the sacrificial oxidation step of Tsai et al unnecessary." Examiner's Answer, page 6. The Examiner further asserts, "[i]t would have been within the scope of one of ordinary skill in the art to combine the teachings of Lancaster with those of Tsai et al to protect the trench surfaces of Tsai during removal of the nitride layer 34 in the process of Tsai et al to further provide trench wall surface that are free from damage." Examiner's Answer, page 4.

Apparently, however, that was not the case. Despite the fact that Tsai issued from an application that was filed much later than (about ten years after) the application from which Lancaster issued, and most likely due to stark differences between trench transistors and STI structures, removal of silicon from the surfaces of the STI trenches of Tsai in 1996 was apparently not of as great a concern as removal of silicon from the surfaces of a transistor gate trenches of Lancaster in 1986.

Furthermore, the *sacrificial* oxide layer 52a of Lancaster is unsuitable for use in the final transistor gate structure and, therefore, must be removed. It is initially replaced with a gate oxide layer 57 (FIG. 5F; col. 3, lines 54-58) or 72 (FIG. 7A; col. 5, lines 16-19). Even the majority of the gate oxide layer 57, 72 is subsequently patterned and replaced with dielectric 75 (FIGS. 5K and 5L; col. 4, lines 45-46 and 48-50) or 79 (FIGS. 7E and 7F; col. 5, lines 56-64). The side wall

oxidation 39 of Tsai is, in contrast, formed after removal of silicon nitride and, as depicted in FIG. 3J of Tsai, remains in place in the final STI structure.

While the Examiner asserts that "that removal of silicon from the trenches would be prevented," application of the teachings of Lancaster to the process of Tsai would also require that any oxide on the surfaces of the trench of Tsai be removed, which would also remove material from the pad oxide layer 32A of Tsai. Thus, it is respectfully submitted that one of ordinary skill in the art would have no reason to expect that a combination of teachings from Tsai and Lancaster would be successful.

Additionally, it is respectfully submitted that the references teach away from the asserted combination. Lancaster teaches complete removal of a silicon nitride layer prior to filling trenches. This teaching is inconsistent with Tsai's teaching that a silicon nitride layer remain in place until after trenches are filled to "act[] as an end point detecting layer during [a] CMP process" in which dielectric, trench-filling material that overlies the plane of the silicon nitride layer is removed. Tsai, col. 3, lines 51-56; FIG. 3G.

It is, therefore, respectfully submitted that the teachings of Tsai and Lancaster do not support a *prima facie* case of obviousness against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37. Accordingly, under 35 U.S.C. § 103(a), each of these claims is drawn to subject matter which is allowable over the teachings of Tsai and Lancaster, taken either separately or together.

2. TSAI, LANCASTER, AND THE EXAMINER'S COMMENT

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over that taught in Tsai, in view of the teachings of Lancaster and, further, in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, for depending indirectly from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, for depending indirectly from claim 33, which is allowable.

3. TSAI, LANCASTER, AND LEE

Claims 5, 15, 28, and 36 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that the subject matter taught in Tsai, in view of teachings from Lancaster and, further, in view of the teachings of Lee, HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59.

Claims 5, 15, 28, and 36 are allowable, among other reasons, for depending directly from claims 1, 11, 25, and 33, respectively, which are allowable.

(XI) CONCLUSION

It is respectfully submitted that each of claims 1-20 is directed to subject matter that, under 35 U.S.C. § 102(b), is allowable over the subject matter described in Simko.

Accordingly, it is respectfully requested that the rejections of claims 1-20 be reversed, and that each of these claims be allowed.

Respectfully submitted,

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